

# RV64i Base Integer Instructions

Opcode	Instruction	Fmt	Example	Description	Notes	
li	load immediate	*	li a0, 2	addi a0, zero, 2	<i>pseudo</i>	
la	load address	*	la a0, symbol	a0 = symbol	<i>pseudo</i> , 2 instr	
add	add	R	add a0, a1, a2	a0 = a1 + a2	sign-extends	
sub	subtract	R	sub a0, a1, a2	a0 = a1 - a2		
xor	bitwise exclusive or	R	xor a0, a1, a2	a0 = a1 ^ a2		
or	bitwise or	R	or a0, a1, a2	a0 = a1   a2		
and	bitwise and	R	and a0, a1, a2	a0 = a1 & a2		
sll	shift left logical	R	sll a0, a1, a2	a0 = a1 << a2		
srl	shift right logical	R	srl a0, a1, a2	a0 = a1 >> a2		
sra	shift right arith*	R	sra a0, a1, a2	a0 = a1 >> a2		
slt	set less than	R	slt a0, a1, a2	a0 = (a1 < a2) ? 1 : 0	unsigned	
sltu	set less than (u)	R	sltu a0, a1, a2	a0 = (a1 < a2) ? 1 : 0		
addi	add immediate	I	addi a0, a1, 2	a0 = a1 + 2	sign-extends	
xori	xor immediate	I	xori a0, a1, 2	a0 = a1 ^ 2		
ori	or immediate	I	ori a0, a1, 2	a0 = a1   2		
andi	and immediate	I	andi a0, a1, 2	a0 = a1 & 2		
slli	shift left logical imm	I	slli a0, a1, 2	a0 = a1 << 2		
srl	shift right logical imm	I	srl a0, a1, 2	a0 = a1 >> 2		
srai	shift right arith imm	I	srai a0, a1, 2	a0 = a1 >> 2		
slti	set less than imm	I	slti a0, a1, 2	a0 = (a1 < 2) ? 1 : 0		
sltiu	set less than imm (u)	I	sltiu a0, a1, 2	a0 = (a1 < 2) ? 1 : 0	unsigned	
mv	move (copy)	*	mv a0, a1	addi a0, a1, 0	<i>pseudo</i>	
neg	2s-complement negation	*	neg a0, a1	sub a0, zero, a1	<i>pseudo</i>	
not	bitwise not	*	not a0, a1	xori a0, a1, -1	<i>pseudo</i>	
lb	load byte	I	lb a0, 1(a1)	a0 = M[a1+1] (8 bits)	zero-extends	
lh	load half	I	lh a0, 2(a1)	a0 = M[a1+2] (16 bits)		
lw	load word	I	lw a0, 4(a1)	a0 = M[a1+4] (32 bits)		
ld	load double word	I	ld a0, 8(a1)	a0 = M[a1+8] (64 bits)		
lbu	load byte (u)	I	lbu a0, 1(a1)	a0 = M[a1+1] (8 bits)		zero-extends
lhu	load half (u)	I	lhu a0, 2(a1)	a0 = M[a1+2] (16 bits)		zero-extends
lwu	load word (u)	I	lwu a0, 4(a1)	a0 = M[a1+4] (32 bits)		zero-extends
l{b h w d}	load global	*	ld a0, symbol	a0 = M[symbol]	<i>pseudo</i> , 2 instr	
sb	store byte	S	sb a0, 1(a1)	M[a1+1] = a0 (8 bits)	<i>pseudo</i> , 2 instr	
sh	store half	S	sh a0, 2(a1)	M[a1+2] = a0 (16 bits)		
sw	store word	S	sw a0, 4(a1)	M[a1+4] = a0 (32 bits)		
sd	store double word	S	sd a0, 8(a1)	M[a1+8] = a0 (64 bits)		
s{b h w d}	store global	*	sd a0, symbol, t0	M[symbol] = a0 (uses t0)		
beq	branch if =	B	beq a0, a1, 2b	if (a0 == a1) goto 2b	<i>pseudo</i>	
bne	branch if ≠	B	bne a0, a1, 2f	if (a0 != a1) goto 2f		
blt	branch if <	B	blt a0, a1, 2b	if (a0 < a1) goto 2b		
ble	branch if ≤	*	ble a0, a1, 2f	bge a1, a0, 2f		
bgt	branch if >	*	bgt a0, a1, 2b	blt a1, a0, 2b		
bge	branch if ≥	B	bge a0, a1, 2f	if (a0 >= a1) goto 2f		
bltu	branch if < (u)	B	bltu a0, a1, 2b	if (a0 < a1) goto 2b		
bleu	branch if ≤ (u)	*	bleu a0, a1, 2f	bgeu a1, a0, 2f		
bgtu	branch if > (u)	*	bgtu a0, a1, 2b	bltu a1, a0, 2b	unsigned, <i>pseudo</i>	
bgeu	branch if ≥ (u)	B	bgeu a0, a1, 2f	if (a0 >= a1) goto 2f	unsigned	
beqz	branch if = 0	*	beqz a0, 2b	if (a0 == 0) goto 2b	<i>pseudo</i>	
bnez	branch if ≠ 0	*	bnez a0, 2f	if (a0 != 0) goto 2f	<i>pseudo</i>	
bltz	branch if < 0	*	bltz a0, 2b	if (a0 < 0) goto 2b	<i>pseudo</i>	
blez	branch if ≤ 0	*	blez a0, 2f	if (a0 ≤ 0) goto 2f	<i>pseudo</i>	
bgtz	branch if > 0	*	bgtz a0, 2b	if (a0 > 0) goto 2b	<i>pseudo</i>	
bgez	branch if ≥ 0	*	bgez a0, 2f	if (a0 ≥ 0) goto 2f	<i>pseudo</i>	
jal	jump and link	J	jal ra, label	ra = pc+4; jump to label		
jalr	jump and link reg	I	jalr ra, a1	ra = pc+4; jump to a1		
call	call subroutine	*	call label	ra = pc+4; jump to label		
j	jump	*	j label	jump to label		
lui	load upper imm	U	lui a0, 1234	a0 = 1234 << 12		
auipc	add upper imm to pc	U	auipc a0, 1234	a0 = pc + (1234 << 12)		
ecall	environment call	I	ecall	system call (calls the OS)		
ebreak	environment break	I	ebreak	break to debugger		

## RV64m Multiply Extension

Opcode	Instruction	Fmt	Example	Description	Notes
<code>mul</code>	multiply	R	<code>mul a0, a1, a2</code>	$a0 = a1 * a2$	
<code>mulh</code>	multiply high	R	<code>mulh a0, a1, a2</code>	$a0 = a1 * a2$ (high bits)	
<code>mulsu</code>	multiply high (s*u)	R	<code>mulsu a0, a1, a2</code>	$a0 = a1 * a2$ (high bits)	a1 signed, a2 unsigned
<code>mulu</code>	multiply high (u)	R	<code>mulu a0, a1, a2</code>	$a0 = a1 * a2$ (high bits)	unsigned
<code>div</code>	divide	R	<code>div a0, a1, a2</code>	$a0 = a1 / a2$	
<code>divu</code>	divide (u)	R	<code>divu a0, a1, a2</code>	$a0 = a1 / a2$	unsigned
<code>rem</code>	remainder	R	<code>rem a0, a1, a2</code>	$a0 = a1 \% a2$	
<code>remu</code>	remainder (u)	R	<code>remu a0, a1, a2</code>	$a0 = a1 \% a2$	unsigned

## Registers

Register	ABI Name	Description	Saver
<code>x0</code>	<code>zero</code>	Zero constant	—
<code>x1</code>	<code>ra</code>	Return address	Caller
<code>x2</code>	<code>sp</code>	Stack pointer	Callee
<code>x3</code>	<code>gp</code>	Global pointer	—
<code>x4</code>	<code>tp</code>	Thread pointer	—
<code>x5-x7</code>	<code>t0-t2</code>	Temporaries	Caller
<code>x8</code>	<code>s0 / fp</code>	Saved / frame pointer	Callee
<code>x9</code>	<code>s1</code>	Saved register	Callee
<code>x10-x11</code>	<code>a0-a1</code>	Fn args/return values	Caller
<code>x12-x17</code>	<code>a2-a7</code>	Fn args	Caller
<code>x18-x27</code>	<code>s2-s11</code>	Saved registers	Callee
<code>x28-x31</code>	<code>t3-t6</code>	Temporaries	Caller

## Core Instruction Formats

31	27	26	25	24	20	19	15	14	12	11	7	6	0	
funct7			rs2		rs1		funct3		rd		opcode			R-type
imm[11:0]					rs1		funct3		rd		opcode			I-type
imm[11:5]			rs2		rs1		funct3		imm[4:0]		opcode			S-type
imm[12 10:5]			rs2		rs1		funct3		imm[4:1 11]		opcode			B-type
imm[31:12]									rd		opcode			U-type
imm[20 10:1 11 19:12]									rd		opcode			J-type